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EXAMINER	
AHMED, SALMAN	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,085	GOETZINGER ET AL.	
	Examiner	Art Unit	
	Salman Ahmed	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/24/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-24* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/1/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-24 are pending

Claims 1-9, 11-24 are rejected

Claim 10 is objected.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 5, 8, 13, 16, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meier et al. (U.S. 6,481,251), hereinafter referred to as Meier, in view of Gupta et al. (US PAT 7027394), hereinafter referred to as Gupta.

Regarding claims 5, 8, 13 and 16 Meier teaches "examining an empty indicator associated with the scheduling queue;" Meier teaches empty indication for store queue as as described in column 13, lines 66-67 and column 14, lines 1-4; "refraining from searching the scheduling queue if the empty indicator indicates that the scheduling queue is empty; searching the scheduling queue if the empty indicator indicates that the scheduling queue is not empty; detaching from the scheduling queue a winning flow found in the searching step." Meier teaches store queue control circuit 74 generates a mask using the load's store queue number and the head store queue number (step 120). The mask includes a bit for each store queue entry. The bit is set if the store queue entry is eligible to be hit by the load (i.e. the entry is between the head entry indicated by the head store queue number and the entry indicated by the load's store queue number), and is clear if the store queue entry in not eligible to be hit by the load. As stated in column 14, lines 60-67. In other words, store queue control circuit 74 determines if there is still a hit signal asserted after masking via step 122. If so, data is forward to D-cache 44 from the hit entry (step 126). As stated in column 15, lines 7-10.

Regarding claim 24, Meier teaches all the limitations of claim 24 as discussed with claim 13. It should be noted that claim 24 is simply the computer program containing the methods of claim 13.

Regarding claim 22, Meier teaches all the limitations of claim 22 as discussed with claim 5. It should be noted that claim 22 is simply the computer program containing the methods of claim 5 (The reference teaches in column 2 lines 55-59, a computer system is contemplated including the processor and an input/output (I/O) device

configured to communicate between the computer system and another computer system to which the I/O device is couplable).

Meier does not explicitly teach a plurality of empty indicators associated with the scheduling queues.

Gupta in the same field of endeavor teaches a plurality of queue having corresponding empty indicators (column 34 lines 33-50 and figure 29, 30, 32 and 34, If the FC flag is ON, the scheduler checks at 922 whether the corresponding queue is empty (empty flag or indicator or some indication of absence of data). If the queue is empty, or if the FC flag is OFF, the priority counter is incremented. If the queue is not empty, the scheduler checks at 924 whether the token bucket for that queue has enough credits).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Meier's teaching by incorporating the steps of using a plurality of empty indicators as taught by Gupta. The motivation is that such method would save cpu processing time and resources by not executing read cycle on an empty queue; thus making the network efficient.

4. Claims 9, 11, 12 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naven et al. (U.S. 6,810,043), hereinafter referred to as Naven in view of Gupta.

Regarding claim 9, Naven teaches "attaching a flow to the scheduling queue" Naven teaches each storage location 2 is capable of storing one or more entries, each such entry denoting that a specified virtual channel is to be serviced by the traffic

manager in the time slot which the storage location corresponds as stated in column 1, lines 58-61. "Placing an empty indicator associated with the scheduling queue in a condition to indicate that the scheduling queue is not empty." Naven discloses the master snoop memory 20 is N bits wide such that each N-bit word 22 corresponds individually to one of the storage locations 2 of the group. In this case, when a bit in the word 22 is set to 1, this denotes that the corresponding storage location 2 has at least one VC entered therein.

Naven does not explicitly teach a plurality of empty indicators associated with the scheduling queues.

Gupta in the same field of endeavor teaches a plurality of queue having corresponding empty indicators (column 34 lines 33-50 and figure 29, 30, 32 and 34, If the FC flag is ON, the scheduler checks at 922 whether the corresponding queue is empty. If the queue is empty (empty flag or indicator or some indication of absence of data), or if the FC flag is OFF, the priority counter is incremented. If the queue is not empty, the scheduler checks at 924 whether the token bucket for that queue has enough credits)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Naven's teaching by incorporating the steps of using a plurality of empty indicators as taught by Gupta. The motivation is that such method would save cpu processing time and resources by not executing read cycle on an empty queue; thus making the network efficient.

Regarding claim 11, "setting a bit in a register" Naven teaches when a bit in the word 22 is set to 1, this denotes that the corresponding storage location 2 has at least one VC entered therein (column 8, lines 24-26).

Regarding claim 12, "resetting a bit in a register" Naven teaches if the bit is 0, on the other hand, this denotes that the corresponding storage location 2 is "empty", i.e. does not contain a valid entry (column 8, lines 26-28).

Regarding claim 23, Naven teaches all the limitations of claim 23 as discussed with claim 9. It should be noted that claim 23 is simply the computer program containing the methods of claim 9.

5. Claims 1-4,19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figure 1,2 and 3 in view of Meier, further in view of Gupta.

Regarding claim 1, "network processor, comprising:" Applicant's admitted Prior Art Figure 1 teaches network processor (28,30) "one or more schedules queues, each adapted to define a respective sequence in which flows are to be serviced". Admitted Prior Art Figure 2 teaches scheduler queue and sequence of data flow 42.

Admitted Prior Art fails to explicitly teach one or more empty indicators, each empty indicator being associated with a respective scheduling queue to indicate whether the respective scheduling queue is empty.

However, Meier in the same field of endeavor teaches empty indication in the empty indicator in schedule queue in order to indicate whether the respective

scheduling queue is empty as described in column 14, lines 2-4 of Meier et al. reference.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Applicant's admitted prior art by incorporating the steps of using a empty indicators as taught by Meier. The motivation is that such method would save cpu processing time and resources by not executing read cycle on an empty queue; thus making the network efficient.

Regarding claim 2, Admitted Prior Art fails to explicitly teach empty indication may be a bit indicating empty when set and indicating not empty when clear.

Meier et al. in the same field of endeavor teaches empty indication may be a bit indicating empty when set and indicating not empty when clear, as stated in column 14, lines 5-6.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Applicant's admitted prior art by incorporating the steps of setting/unsetting a empty indicators as taught by Meier. The motivation is that such method would save cpu processing time and resources by not executing read cycle on an empty queue; thus making the network efficient.

Regarding claim 19, "network processor, comprising:" Applicant's admitted Prior Art Figure 1 teaches network processor (28,30) "one or more scheduling queues, each adapted to define a respective sequence in which flows are to be serviced". Admitted Prior Art Figure 2 teaches scheduler queue and sequence of data flow 42.

Admitted Prior Art fails to explicitly teach "one or more empty indicators, each empty indicator being associated with a respective scheduling queue to indicate whether the respective scheduling queue is empty." Admitted Prior Art fails to explicitly teach "examining an empty indicator associated with the first scheduling queue"

However, Meier in the same field of endeavor teaches empty indication in the empty register indicates that the store queue is empty. Column 14, lines 2-3 Meier in the same field of endeavor teaches empty indication for store queue as spoken of column 13, lines 66-67 and column 14, lines 1-4 "refraining from searching the first scheduling queue if the empty indicator indicates that the first scheduling queue is empty; searching the first scheduling queue if the empty indicator indicates that the first scheduling queue is not empty; and detach from the first scheduling queue a winning flow found in the search of the first scheduling queue." Meier in the same field of endeavor teaches store queue control circuit 74 generates a mask using the load's store queue number and the head store queue number (step 120). The mask includes a bit for each store queue entry. The bit is set if the store queue entry is eligible to be hit by the load (i.e. the entry is between the head entry indicated bf the head store queue number and the entry indicated by the load's store queue number), and is clear if the store queue entry in not eligible to be hit by the load. As stated in column 14, lines 60-67. In other words, storage queue control circuit! 74 determines if there is still a hit signal asserted after masking via step 122. If so, data is forward to D-cache 44 from the hit entry (step 126). As stated in column 15, lines 7-10. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references

to implement empty indicator of Meier in schedule queue of Admitted prior Art in order to indicate weather the respective scheduling queue is empty as spoken of on column 14, line 2-4 of Meier reference.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Applicant's admitted prior art by incorporating the steps of setting/unsetting a empty indicators as taught by Meier. The motivation is that such method would save cpu processing time and resources by not executing read cycle on an empty queue; thus making the network efficient.

Regarding claim 21, "network processor, comprising:" Applicant's admitted Prior Art Figure 1 teaches network processor (28,30) "one or more scheduling queues each adapted to define a respective sequence in which flows are to be serviced" Admitted Prior Art Figure 2 teaches scheduler queue and sequence of data flow 42.

Admitted Prior Art fails to explicitly teach one or more empty indicators, each empty indicator being associated with a respective scheduling queue to indicate whether the respective scheduling queue is empty. Admitted Prior Art fails to teach "examine an empty indicator associated with a first scheduling queue; refrain from searching the first scheduling queue if the empty indicator indicates that the first scheduling queue is empty; search the first scheduling queue if the empty indicator indicates that the first scheduling queue is not empty; if a winning flow is found by the search of the first scheduling queue, detach the winning flow from the first scheduling queue; if no flow is found by the search of the first scheduling queue, place the empty indicator in a condition to indicate that the first scheduling queue is empty."

However, Meier et al. in the same field of endeavor teaches empty indication in the empty register indicates that the store queue is empty. Column 14, lines 2-3. Meier et al. in the same field of endeavor teaches store queue control circuit 74 generates a mask using the load's store queue number and the head store queue number (step 120). The mask includes a bit for each store queue entry. The bit is set if the store queue entry is eligible to be hit by the load (i.e. the entry is between the head entry indicated by the head store queue number and the entry indicated by the load's store queue number), and is clear if the store queue entry in not eligible to be hit by the load. As stated in column 14, lines 60-67. In other words, store queue control circuit 74 determines if there is still a hit signal asserted after masking via step 122. If so, data is forward to D-cache 44 from the hit entry (step 126). As stated in column 15, lines 7-10.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to implement empty indicator of Meier in schedule queue of Admitted Prior Art in to search or not to search if empty indicator indicate empty or not empty as spoken of on column 14, line 2-6 of Meier et al. reference. The motivation is that such method would save cpu processing time and resources by not executing read cycle on an empty queue; thus making the network efficient.

In regards to claims 1, 19 and 21 Applicant's admitted prior art and Meier do not explicitly teach a plurality of empty indicators.

Gupta in the same field of endeavor teaches a plurality of queue having corresponding empty indicators (column 34 lines 33-50 and figure 29, 30, 32 and 34, If the FC flag is ON, the scheduler checks at 922 whether the corresponding queue is empty. If

the queue is empty, or if the FC flag is OFF, the priority counter is incremented. If the queue is not empty, the scheduler checks at 924 whether the token bucket for that queue has enough credits)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Applicant's admitted prior art and Meier's teaching by incorporating the steps of using a plurality of empty indicators as taught by Gupta. The motivation is that such method would save cpu processing time and resources by not executing read cycle on an empty queue; thus making the network efficient.

Regarding claim 3, Applicant's admitted Prior Art further discloses one or more schedule queues 42 include plurality of scheduling queues as shown in Figure 2. Admitted Prior Art fails to disclose empty indicators include a plurality of empty indicators. However, Meier et al. in the same field of endeavor in Figure 5, illustrates store queue assignment circuit 60 in response to completion of one or more stores. Additionally, store queue number assignment circuit 60 determines if the head store queues number equals the tail store queue number. If so, the empty indication in empty register 65 is set to indicate empty as stated in column 14, lines 24-48. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to use plurality of empty indicators of Meier et al. along with plurality of scheduling queues of Admitted Prior Art Figure 2. A motivation for doing so would be, if the scheduling queue that is searched during a given cycle turns out to be empty, then the cycle may be wasted.

Regarding claim 4, Applicant's admitted Prior Art further discloses each scheduling queue 42 includes 512 slots 48 to which flows are attachable as shown in Figure 2 and 3.

6. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meier in view Gupta as applied to claim 13 above and further in view of Naven.

In regards to claims 17 and 18 Meier and Gupta teach queue scheduling method as described in the rejections of claim 13 above.

In regards to claim 17, Meier and Gupta do not explicitly teach detaching step is performed, a further search of the scheduling queue is performed to determine whether any flows are enqueued in the scheduling queue other than the flow detached in the detaching step.

Naven in the same field of endeavor discloses if the detaching step is performed, a further search of the scheduling queue is performed to determine whether any flows are en-queued in the scheduling queue other than the flow detached in the detaching step' (Column 8, lines 24-28, when a bit in the word 22 is set to 1 this denotes that the corresponding storage location 2 has at least one VC entered therein. If the bit is 0, on the other hand, this denotes that the corresponding storage location 2 is "empty" i.e. does not contain a valid entry).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Meier and Gupta's method by incorporating the method of doing further search and setting an indicator as taught by Naven. The motivation is that such

additional search will help prevent race condition, i.e. during first search if the state of the queue changes, it will be detected; thus making the system more robust and less error prone.

In regards to claims 18, Meier and Gupta do not explicitly teach empty indicator is placed in a condition to indicate that the scheduling queue is empty if the further search of the scheduling queue determines that there are no flows in the scheduling queue other than the flow detached in the detaching step.

Regarding claim 18, Naven in the same field of endeavor discloses "the empty indicator is placed in a condition to indicate that the scheduling queue is empty if the further search of the scheduling queue determines that there are no flows in the scheduling queue other than the flow detached in the detaching step (column 8, lines 26-28, if the bit is 0, on the other hand, this denotes that the corresponding storage location 2 is "empty", i.e. does not contain a valid entry).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Meier and Gupta's method by incorporating the method of doing further search and setting an indicator as taught by Naven. The motivation is that such additional search will help prevent race condition, i.e. during first search if the state of the queue changes, it will be detected; thus making the system more robust and less error prone.

7. Claims 6 and14 rejected under 35 U.S.C. 103(a) as being unpatentable over Meier in view of Gupta as applied to claims 5 and 13 above, further in view of Lyons et

al. (Third New Zealand ATM and Broadband Workshop: Title- Estimating Clock Speeds for the ATMSWITCH Architecture).

Regarding claims 6 and 14, Meier and Gupta teach plurality of empty indicator associated with scheduling queue, refraining from searching the scheduling queue if the empty indicator indicates empty, and searching the scheduling queue if the empty indicator indicates non-empty (see claim 5 and 13).

Meier and Gupta do not explicitly teach, selecting the scheduling queue from among a plurality of scheduling queues in a round robin process.'

Lyons et al. in the same field of endeavor teaches round robin process in ATMSWITCH (Column 3, Paragraph 4 lines 6-11).

At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to implement empty indicator of Meier and Gupta and searching the scheduling queue in a round robin server as in Lyons et al. in moves around the circular queue removing a cell from the current cell queue whenever the output port becomes free, and moving on to next queue in time for the next output slot. Column 3, Paragraph 4 lines 6-11 under The ATMSWITCH. Round-Robin process lets all queues get fair scheduling and helps efficient transmission of data.

8. Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meier in view of Gupta as applied to claims 5 and 13 above, further in view of Naven.

Regarding claim 7 and 15, Meier and Gupta teach plurality of empty indicators associated with scheduling queue, refraining from searching the scheduling queue if the

empty indicator indicates empty, and searching the scheduling queue if the empty indicator indicates non-empty (see claims 5 and 13).

Meier and Gupta do not explicitly teach "searching step includes a plurality of sub-queues includes in the scheduling queue, the sub-queues having mutually different respective ranges and resolutions."

Naven in the same field of endeavor teaches that the master calendar (scheduling queue) and slave calendar (sub-queues) are plurality of storage locations corresponding respectively to a succession of time slots (column 4 lines 44-45). It can also be seen from figure 2 that the slave calendar and master calendar have a different number of time slots.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Meier and Gupta's method by incorporating the method of having different ranges and resolutions for sub-queues as taught by Naven. A motivation for doing so would be the master calendar and slave calendar have the different range and resolution of slots (the scheduling queue has different number of slots that is different than a number slots of the sub-queue, 7 and 2 of figure 2). This would make the system hierarchal and would help implement efficient network management.

9. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art Figure 1,2 and 3 in view of Meier in view of Naven in view of Gupta.

Regarding claim 20, "network processor, comprising:" Applicant's admitted Prior Art Figure 1 teaches network processor (28,30) "one or more scheduling queues, each adapted to define a respective sequence in which flows are to be serviced". Admitted Prior Art Figure 2 teaches scheduler queue and sequence of data flow 42.

Admitted Prior Art fails to explicitly teach "one or more empty indicators, each empty indicator being associated with a respective scheduling queue to indicate whether the respective scheduling queue is empty."

However, Meier et al. in the same field of endeavor teaches empty indication in the empty register indicates that the store queue is empty (Column 14, lines 2-3).

At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to implement empty indicator of Meier in schedule queue of Admitted Prior Art in order to indicate whether the respective scheduling queue is not empty as spoken of on column 14, line 2-6 of Meier et al. reference. A motivation for doing so would be, if the scheduling queue that is searched during a given cycle turns out to be empty, than the cycle may be wasted.

Admitted Prior Art and Meier et al. fails to teach "attach a flow to the first scheduling queue".

Naven teaches each storage location 2 is capable of storing one or more entries, each such entry denoting that a specified virtual channel is to be serviced by the traffic manager in the time slot which the storage location corresponds as stated in column 1, lines 58-61; place an empty indicator associated with the first scheduling queue in a condition to indicate that the first scheduling queue is not empty." Naven discloses the

master snoop memory 20 is N bits wide such that each N-bit word 22 corresponds individually to one of the storage locations 2 of the group. In this case, when a bit in the word 22 is set to 1, this denotes that the corresponding storage location 2 has at least one VC entered therein.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to implement empty indicator of Applicant's Admitted Prior art and Meier with attaching a flow to the first scheduling queue as taught by Naven. A motivation for doing so would be, if the scheduling queue that is searched during a given cycle in not empty, than the cycle may be not wasted by attaching appropriate task or flow to that queue; thus making the resources efficiently utilized.

Applicant's admitted prior art, Meier and Naven do not explicitly teach a plurality of empty indicators.

Gupta in the same field of endeavor teaches a plurality of queue having corresponding empty indicators (column 34 lines 33-50 and figure 29, 30, 32 and 34, If the FC flag is ON, the scheduler checks at 922 whether the corresponding queue is empty. If the queue is empty, or if the FC flag is OFF, the priority counter is incremented. If the queue is not empty, the scheduler checks at 924 whether the token bucket for that queue has enough credits)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Applicant's admitted prior art, Meier and Naven's teaching by incorporating the steps of using a plurality of empty indicators as taught by Gupta. The

motivation is that such method would save cpu processing time and resources by not executing read cycle on an empty queue; thus making the network efficient.

Allowable Subject Matter

10. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

11. Applicant's arguments, pages 11-19 of the Remarks section, filed 7/24/2006, with respect to the rejections of claims 1-9 and 11-24 have been fully considered and are not persuasive.

Applicant has amended the independent claims 1, 5, 9, 13 and 19-24 by adding the limitation "...a plurality of empty indicators..."; thus changing the scope of the claims. Applicant's amendment necessitated a new ground of rejections presented in this office action. As such, any response to the arguments of the Applicant regarding rejections of claims 1-9 and 11-24 is moot.

Applicant argues in page 12 paragraph two that the Applicant's invention is a network processor environment, while Meier discloses a computer processor. However, the Examiner respectfully points out that the network processor is a processor used in a network environment. Meier teaches a computer system is contemplated including the

processor and an input/output (I/O) device configured to communicate between the computer system and another computer system to which the I/O device is couplable (column 2 lines 55-59). As such Examiner respectfully disagrees with the Applicant on this issue. Applicant further argues the present invention relates to a network processor, which operates to make connection and assign limited bandwidth fairly and efficiently in order to transmit data over relatively large distances. There is no user program running at all. Instead, the plurality of empty indicators of the present invention provide a mechanism for determining which scheduling queue should be serviced in the next pass. However Examiner respectfully points out that such limitation, although disclosed, is not reflected in the claim.

Applicant argues (see page 12 last paragraph) that Meier does not disclose a method of dequeuing a flow from a scheduling queue as recited in claim 5. However, Examiner respectfully disagrees with this assertion. Meier does teach the cited limitation. Meier further teaches If a hit on a store queue entry, is detected, the corresponding store queue data is read and provided to D-cache 44 for forwarding (store forward data in FIG. 3 and column 11 lines 54-56).

Applicant argues (see page 13 first paragraph) that Meier cannot anticipate claim 5 because the methods of servicing and dequeuing a flow according to the present invention do not involve the processing described by Meier. However, Examiner respectfully disagrees with this assertion. The present claim language is broad and in view of the broadest reasonable interpretation of this language, Meier does in fact disclose the ignoring steps as described in the rejection of claim 5 in the office action.

Applicant argues (see page 13 second paragraph) that claim 13 is patentable for same reasons as described above. However, Examiner disagrees with the assertion for the same reasons cited above.

Applicant has amended the independent claims 22 (page 13 last paragraph) and 23 (page 14, second paragraph), by adding the limitation "...a plurality of empty indicators..."; thus changing the scope of the claims. Applicant's amendment necessitated a new ground of rejections presented in this office action. As such, any response to the arguments of the Applicant regarding rejections of claims 22 and 24 is moot.

Applicant has amended the independent claims 9 (page 14 last paragraph) and 23 (page 15, second paragraph), by adding the limitation "...a plurality of empty indicators..."; thus changing the scope of the claims. Applicant's amendment necessitated a new ground of rejections presented in this office action. As such, any response to the arguments of the Applicant regarding rejections of claims 9 and 23 is moot.

Applicant has amended the independent claims 1 (page 15 last paragraph) 19 (page 16, second paragraph) and 21 (page 16, third paragraph), by adding the limitation "...a plurality of empty indicators..."; thus changing the scope of the claims. Applicant's amendment necessitated a new ground of rejections presented in this office action. As such, any response to the arguments of the Applicant regarding rejections of claims 1, 19 and 21 is moot.

Dependent claims 2-4, 6-9, 11, 12, 14-18 depend on amended

independent claims 1, 5, 9 and 13. Since Applicant has amended the independent claims 1, 5, 9, 13 and 19-24 by adding the limitation "...a plurality of empty indicators.."; thus changing the scope of the independent claims. Applicant's amendment necessitated a new ground of rejections presented in this office action. As such, Examiner respectfully disagrees with the Applicant about the allowability of claims 2-4, 6-9, 11, 12, 14-18 as they depend on rejected base claims 1, 5, 9 and 13 presented in this office action.

Applicant has amended the independent claims 20 by adding the limitation "...a plurality of empty indicators.."; thus changing the scope of the claim. Applicant's amendment necessitated a new ground of rejection presented in this office action. As such, any response to the arguments (see page 16 paragraph two) of the Applicant regarding rejections of claims 20 is moot.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Salman Ahmed whose telephone number is (571)272-8307. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Art Unit 2616

SA
8/8/2006

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
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